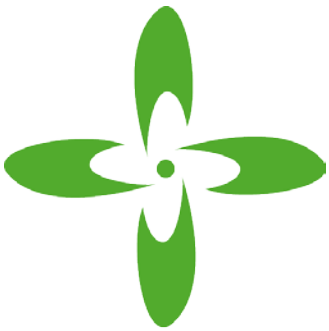

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TM8761

DATA SHEET

Rev 1.0

AMENDMENT HISTORY

Version	Date	Description
V1.0	2019/04/29	New release

CONTENTS

GENERAL DESCRIPTION

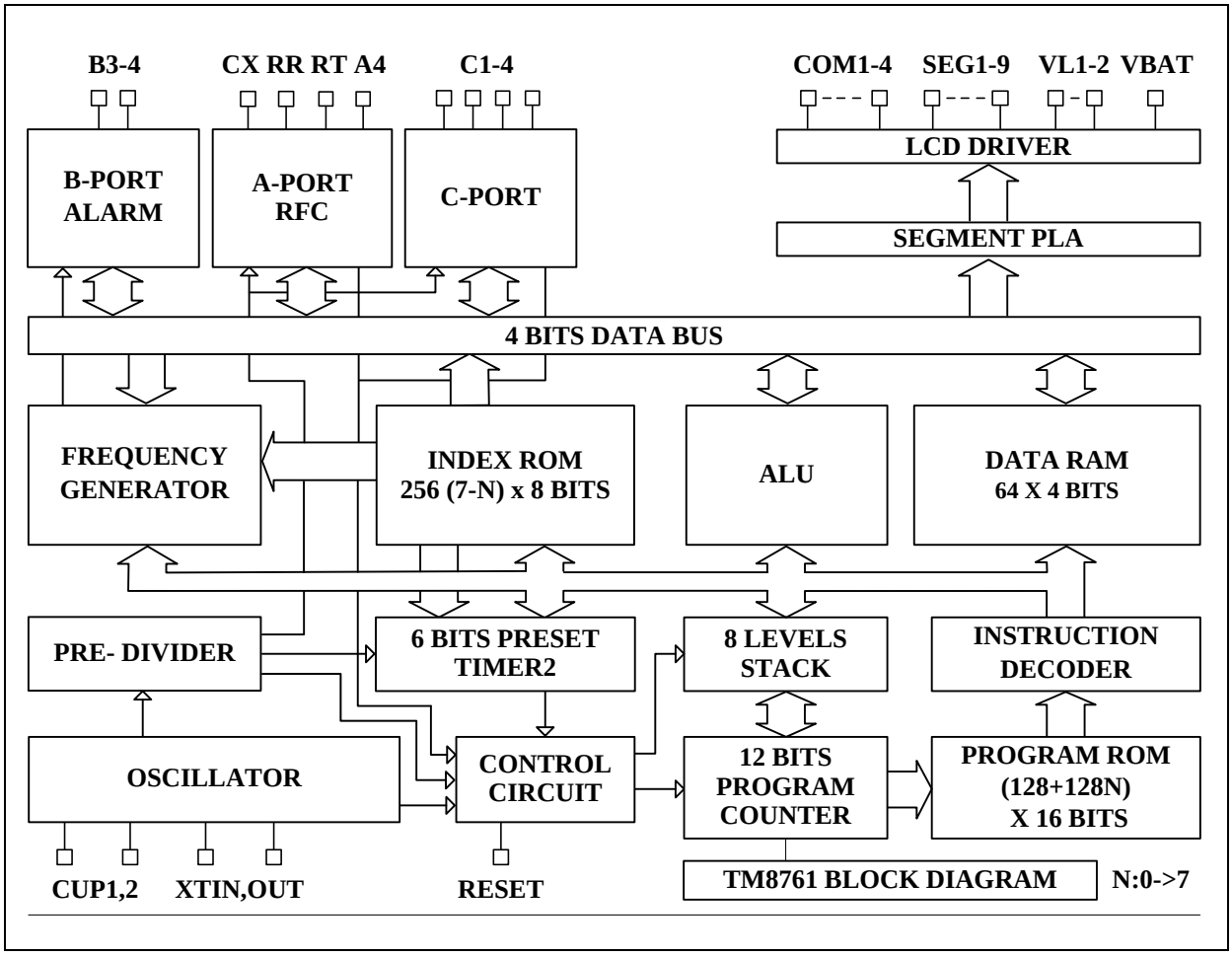
The TM8761 is an embedded high-performance 4-bit microcomputer with LCD driver. It contains all the of the following functions in a single chip: 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter (RFC), LCD driver, look-up table.

FUNCTION

1. **Powerful instruction set (137 instructions)**
   - Binary addition, subtraction, BCD adjustment, logical operation in direct and index addressing mode.
   - Single-bit manipulation (set, reset, decision for branch).
   - Various conditional branches.
   - 16 working registers and manipulation.
   - Look-up table.
   - LCD driver data transfer.
2. **Memory capacity**
   - ROM capacity 1024 x 16 bits.
   - RAM capacity 64 x 4 bits.
3. **Input/output ports**
   - Port IOA4 1 pin (with internal pull-low).
     IOA4 port has built-in input signal chattering prevention circuitry.
   - Port IOC 4 pins (with internal pull-low, low-level-hold).
   - Port IOB3, 4 2 pins (with internal pull-low), & mask option with BZB, BZ.
4. **8-level subroutine nesting.**
5. **Interrupt function**
   - External factor 1 (Pin IOA4 port).
   - Internal factors 3 (Pre-Divider, Timer2 & RFC).
6. **Built-in Alarm, clock or single tone melody generator (BZB, BZ), & mask option with IOB3, 4.**
7. **Built-in R to F Converter circuit**
   - CX, RR, RT.
8. **One 6-bit programmable timer (Timer 2) with programmable clock source.**

9. **LCD driver output**
   - 9 LCD driver outputs (Up to drive 36 LCD segments) .
   - 1/4 Duty and 1/2 Bias for LCD display.
   - Single instruction to turn off all segments.
   - 9 DC/Open Drain outputs for LED mask option.
   - 16 LCD Address.
10. **Built-in Voltage double charge pump circuit.**
11. **Clock oscillation can be defined as X'tal, external-R or internal-R 2 type oscillators by mask option.**
12. **HALT function.**
13. **STOP function.**

BLOCK DIAGRAM



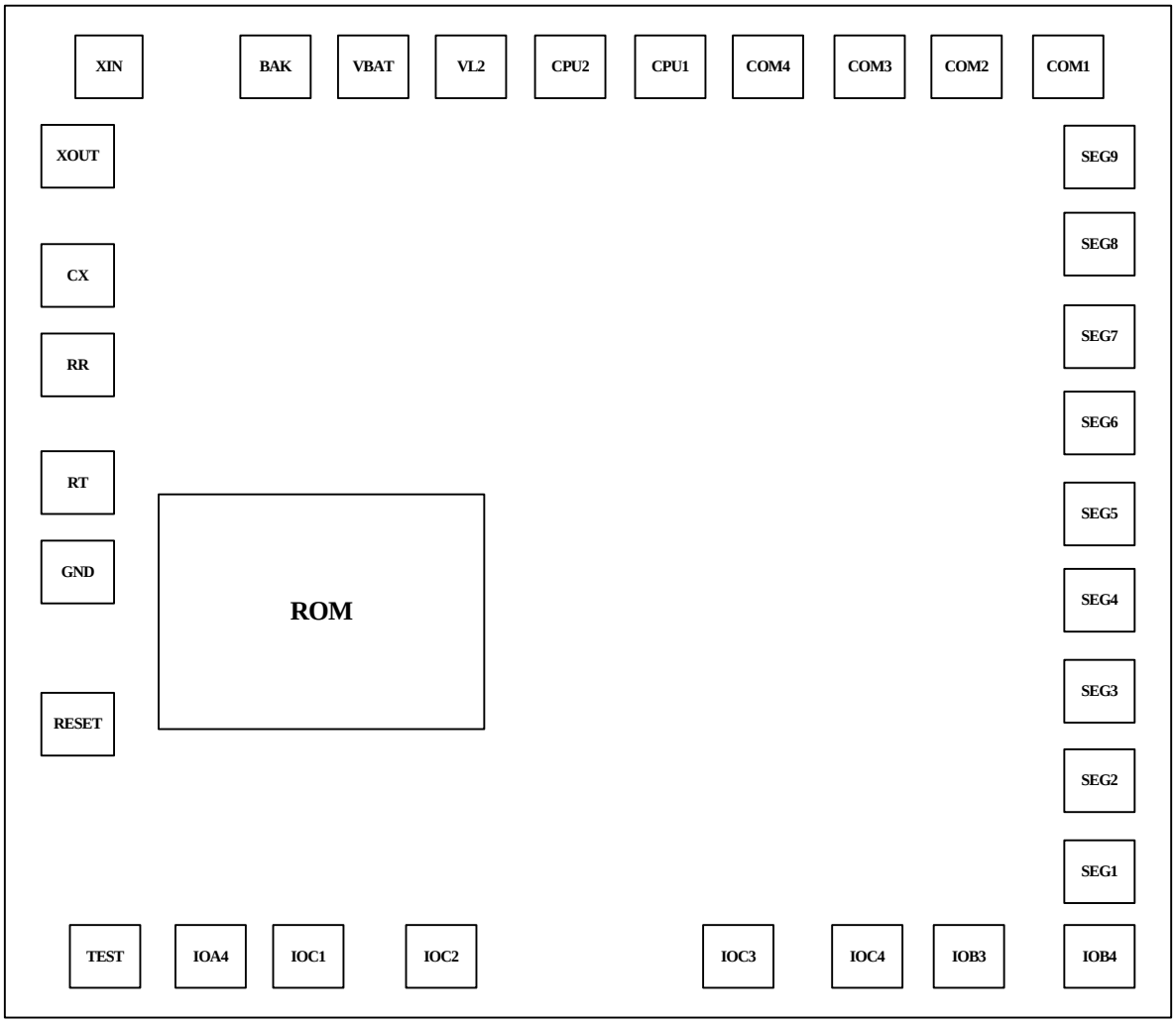
APPLICATION

- Thermometer, Timer

PIN DESCRIPTION

Name	I/O	Description
VBAT	P	Positive power supply. Connect a 0.1 uF capacitor to GND.
BAK (VL1)	P	Internal logic, RFC & LCD mode level1 supply voltage Connected to VBAT.
VL2	P	LCD mode level 2 supply voltage. Connect a 0.1 uF capacitor to GND for LCD mode. Short to VBAT for O/P Mode.
RESET	I	Input pin for chip reset request signal, with internal pull-down resistor.
TEST	I	Test signal input pin.
CUP1, 2	O	Switching pins for supply the LCD driving voltage. Connect the CUP1 and CUP2 pins with a 0.1uf non-polarized capacitor for LCD mode.
COM1~4	O	Output pins for driving the common pins of the LCD panel.
SEG1~9	O	Output pins for driving the LCD panel segment.
IOA4	I/O	I/O port pin.
IOB3, 4	I/O	I/O port pins, & mask option with BZB, BZ
IOC1~4	I/O	I/O port pins
CX RR, RT	I O	1 input pin and 2 output pins for RFC application.
BZB, BZ	O	Output port for alarm, frequency or melody generator
XIN XOUT	I O	System clock oscillation. Connected with 32 KHz crystal oscillator or internal R or external R by mask option.
GND	P	Negative supply voltage.

PAD DIAGRAM



The substrate of chip should be connected to GND.

FUNCTION DESCRIPTION

SRAM

There are 64 X 4 bits data SRAM (40h~7Fh), can be used by direct addressing mode or index addressing mode; the last 16 addresses (70h~7Fh) can be used as Working Register.

ROM

There are 1024 X 16 bits ROM, can be used to divide it for Instruction ROM and Index ROM by mask option. The capacity of Instruction ROM is 128N x 16bits, and the capacity of Index ROM is 256 (8-N) x 8bits (N=1 to 8).

The Index ROM can be used as 4-bits or 8-bits mode.

I/O Ports

The IOC port can be selected by software separately as input or output and with/without internal pull-low.

The IOB3, 4 port can be selected by software separately as input or output and with/without internal pull-low.

The IOA4 port can be selected by software as input or output and with/without internal pull-low and different chattering clock for HALT release /Interrupt trigger to reduce the bounce of key scan:

PH6: 512 Hz PH8: 128 Hz PH10: 32 Hz

The pull-low of IOA4 will be masked off for those pins that are defined as output pins. During developing, the IOA3~1 must be set to output.

The initial state of all I/O Ports are all standard Input state and with internal pull-low resistor.

Before set some pins from input to output, you can execute output function to ensure their output value.

Reset

Reset Pin Reset function. There is no individual “Power On Reset” option because “RESET pin reset” is the only way to start up the program.

When the ‘H’ level signal is applied on the RESET pin, the reset cycle will finish after 64ms automatically, even though the reset signal is longer than 64ms.

Pre-Divider

The pre-divider contains a 15-stage counter using PH0 as clock source; the output of T-Flip-Flop is changed when input clock changes from H to L.

PH11~15 will be reset to L state when power on reset or external reset pin reset or PLC 100 instruction is executed.

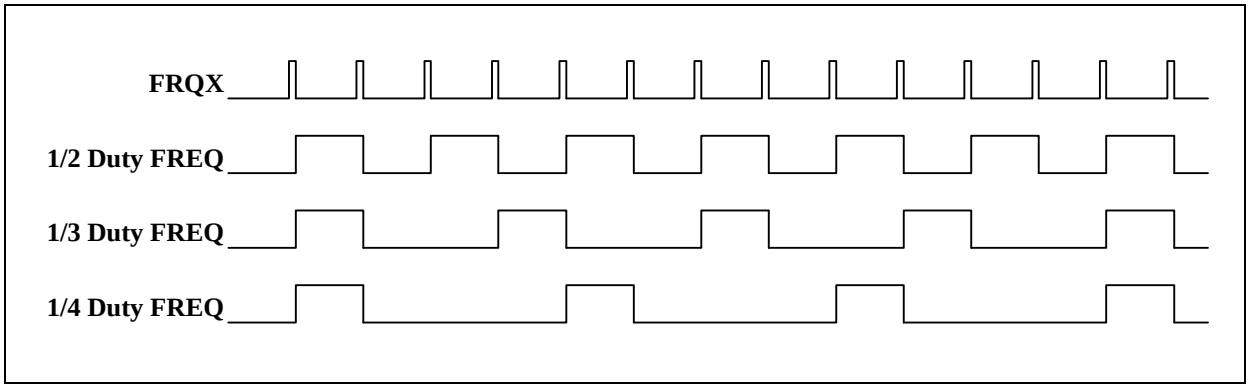
When PH14 is changed from H to L, the HALT release signal HRF3 is generated.

TIMER 2

This 6 bits programmable timer can select PH3/PH9/PH15/FREQ (Timer 2 can also select PH5/PH7 /PH11/PH13 by TM2X instruction) as clock source; when it is underflow, the HALT release signal HRF1/4 is generated.

Alarm/Frequency/Melody

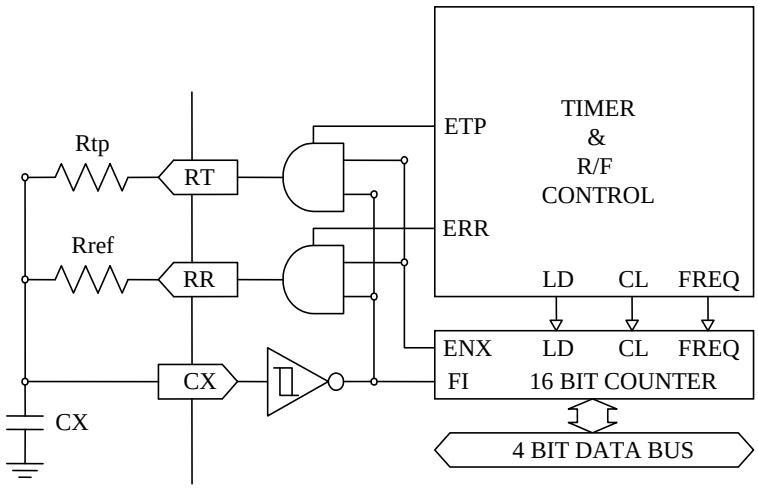
There is an 8-bit programmable counter used as Frequency generator, and a 2-bit control for 1/1,1/2, 1/3 or 1/4 duty selection.



There is another 8-bit envelope control for Alarm, Frequency or Melody output from BZ/BZB.

Resistor to Frequency Converter

There is a Resistor to Frequency Converter; it contains a RC oscillation circuit and a 16-bit counter to calculate relative resistance of temperature or humidity sensor with the reference resistor.



There are two kinds of methodology for measuring the input frequency; first, set CX as clock input and using Timer2 as interval control, or use software directly control the time interval; second, if the CX frequency is too low, either a poor resolution for a fixed interval, or a long period for better resolution but a longer read-out rate, for example, 10 seconds per read-out, in such condition, you can switch the

measuring mode to be setting the CX as interval control, it will enable the counter from the first CX rising edge till next rising edge, then generate a HALT release signal HRF6, and using FREQ (internal frequency generator output) as clock input, hence you can count the interval of CX.

For measuring the resistance of Temperature or Humidity sensor, first we measure the frequency of the Resistor to Frequency Converter, it contains a RC oscillation circuit and a 16-bit counter to calculate relative resistance of temperature and humidity sensor with the reference resistor.

HALT Function

The HALT instruction will disable the system clock and leave only pre-divider, frequency generator, timer and chattering clock for HALT release generation.

STOP Function

The STOP instruction will disable all clocks to minimize the stand-by current (<1 uA).

ABSOLUTE MAXIMUM RATINGS

At Ta= –20°C to 70°C, GND=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VBAT	-0.3 to 3.6	V
	BAK	-0.3 to 3.6	
	VL2	-0.3 to 3.6	
Maximum Input Voltage	Vin	-0.3 to VBAT+0.3	
Maximum output Voltage	Vout1	-0.3 to BAK+0.3	
	Vout2	-0.3 to VL2+0.3	
Maximum Operating Temperature	Topg	-20 to+70	°C°
Maximum Storage Temperature	Tstg	-25 to+125	

ALLOWABLE OPERATING CONDITIONS

At Ta= –20°C to 70°C, GND=0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VBAT	Connected BAK to VBAT	1.2	1.5	1.8	V
	VL2		2xBAKx0.9		2xBAK+0.1	
Input “H” Voltage	Vih1	IOC and IOD port in input mode	VBAT-0.7	-	VBAT+0.7	
Input “L” Voltage	Vil1		-0.7	-	0.7	

ALLOWABLE OPERATING FREQUENCY

At Ta= –20°C to 70°C, GND=0V

Condition	Max. Operating Frequency
BAK=1.5V	800 KHz

ELECTRICAL CHARACTERISTICS INTERNAL RC FREQUENCY RANGE

Option Mode	BAK	Min.	Typical	Max.
350 KHz	1.5V		350 KHz	
650 KHz			650 KHz	

Input Resistance

VBAT=1.5V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
“L” Level Hold Tr. (IOC1~4)	Rllh1	Vi=0.2VBAT	10	40	70	KΩ
IOA4, IOB3~4, IOC1~4 Pull-Down Tr.	Rmad1	Vi=VBAT	200	500	1100	
RES Pull-Down R	Rres1	Vi=GND or VBAT	50	70	100	

DC Output Characteristics

(VL2=1.2V)

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output “H” Voltage	Voh1c	Ioh= -100uA	SEG1~9 , IOB3,4/BZB, BZ, IOC1~4	0.8	0.9	1.0	V
Output “L” Voltage	Vol1c	Iol= 200uA		0.2	0.3	0.4	
Output “H” Voltage	Voh2c	Ioh= -200uA	RR, RT, IOA4	0.8	0.9	1.0	
Output “L” Voltage	Vol2c	Iol= 400uA		0.2	0.3	0.4	

Segment Driver Output Characteristics

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit
1/2 Bias Display Mode							
Output “H” Voltage	Voh12f	Ioh= -1 uA	SEG-n	2.2			V
Output “L” Voltage	Vol12f	Iol= 1 uA				0.2	
Output “H” Voltage	Voh12g	Ioh= -10 uA	COM-n	2.2			
Output “M” Voltage	Vom12g	Iol/h= +/-10 uA	COM-n	1.0		1.4	
Output “L” Voltage	Vol12g	Iol= 10 uA				0.2	

POWER CONSUMPTION

@Ta= –20°C to 70°C, GND=0V, VBAT=1.5V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT	Only 32.768 KHz Crystal oscillator operating, without loading.		2		uA
STOP mode	ISTOP				1	
Operating current	Iop1	RFC operating *	20	45	60	

*** Rtp and Rref=30 KΩ, Cx=0.001 uF**

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

INSTRUCTION TABLE

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz, Ry	0000 0010 ZZZZ YYYY	Lz	← (7SEG ← Ry)	
LCB	Lz, Ry	0000 0100 ZZZZ YYYY	Lz	← (7SEG ← Ry)	Blank Zero
LCP	Lz, Ry	0000 0110 ZZZZ YYYY	Lz	← Ry & AC	
LCD	Lz, @HL	0000 1000 ZZZZ 0000	Lz	← T@HL	
LCT	Lz, @HL	0000 1000 ZZZZ 0001	Lz	← (7SEG ← @HL)	
LCB	Lz, @HL	0000 1000 ZZZZ 0010	Lz	← (7SEG ← @HL)	Blank Zero
LCP	Lz, @HL	0000 1000 ZZZZ 0011	Lz	← @HL & AC	
OPA	Rx	0000 1010 01XX XXXX	PortA (IOA4)	← Rx	Rx: 40~7Fh
OPB	Rx	0000 1100 01XX XXXX	PortB (IOB)	← Rx	
OPC	Rx	0000 1101 01XX XXXX	PortC (IOC)	← Rx	
FRQ	D, Rx	0001 00DD 01XX XXXX	FREQ D=00 D=01 D=10 D=11	← Rx & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D, @HL	0001 01DD 0000 0000	FREQ	←T@HL	
FRQX	D, X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 01XX XXXX	@L	← Rx	Rx: 40~7Fh
MVH	Rx	0001 1101 01XX XXXX	@H	← Rx & AC	
ADC	Rx	0010 0000 01XX XXXX	AC	← Rx + AC + CF	CF, Rx: 40~7Fh
ADC	@HL	0010 0000 1000 0000	AC	← @HL + AC + CF	CF
ADC*	Rx	0010 0001 01XX XXXX	AC, Rx	← Rx + AC + CF	CF, Rx: 40~7Fh
ADC*	@HL	0010 0001 1000 0000	AC, @HL	← @HL + AC + CF	CF
SBC	Rx	0010 0010 01XX XXXX	AC	← Rx + ACB + CF	CF, Rx: 40~7Fh
SBC	@HL	0010 0010 1000 0000	AC	← @HL + ACB + CF	CF
SBC*	Rx	0010 0011 01XX XXXX	AC, Rx	← Rx + ACB + CF	CF, Rx: 40~7Fh
SBC*	@HL	0010 0011 1000 0000	AC, @HL	← @HL + ACB + CF	CF
ADD	Rx	0010 0100 01XX XXXX	AC	← Rx + AC	CF, Rx: 40~7Fh
ADD	@HL	0010 0100 1000 0000	AC	← @HL + AC	CF
ADD*	Rx	0010 0101 01XX XXXX	AC, Rx	← Rx + AC	CF, Rx: 40~7Fh
ADD*	@HL	0010 0101 1000 0000	AC, @HL	← @HL + AC	CF
SUB	Rx	0010 0110 01XX XXXX	AC	← Rx + ACB + 1	CF, Rx: 40~7Fh
SUB	@HL	0010 0110 1000 0000	AC	← @HL + ACB + 1	CF
SUB*	Rx	0010 0111 01XX XXXX	AC, Rx	← Rx + ACB + 1	CF, Rx: 40~7Fh
SUB*	@HL	0010 0111 1000 0000	AC, @HL	← @HL + ACB + 1	CF
ADN	Rx	0010 1000 01XX XXXX	AC	← Rx + AC	Rx: 40~7Fh
ADN	@HL	0010 1000 1000 0000	AC	← @HL + AC	
ADN*	Rx	0010 1001 01XX XXXX	AC, Rx	← Rx + AC	Rx: 40~7Fh
ADN*	@HL	0010 1001 1000 0000	AC, @HL	← @HL + AC	
AND	Rx	0010 1010 01XX XXXX	AC	← Rx AND AC	Rx: 40~7Fh
AND	@HL	0010 1010 1000 0000	AC	← @HL AND AC	

Instruction		Machine Code	Function		Flag/Remark
AND*	Rx	0010 1011 01XX XXXX	AC, Rx	← Rx AND AC	Rx: 40~7Fh
AND*	@HL	0010 1011 1000 0000	AC, @HL	← @HL AND AC	
EOR	Rx	0010 1100 01XX XXXX	AC	← Rx EOR AC	Rx: 40~7Fh
EOR	@HL	0010 1100 1000 0000	AC	← @HL EOR AC	
EOR*	Rx	0010 1101 01XX XXXX	AC, Rx	← Rx EOR AC	Rx: 40~7Fh
EOR*	@HL	0010 1101 1000 0000	AC, @HL	← @HL EOR AC	
OR	Rx	0010 1110 01XX XXXX	AC	← Rx OR AC	Rx: 40~7Fh
OR	@HL	0010 1110 1000 0000	AC	← @HL OR AC	
OR*	Rx	0010 1111 01XX XXXX	AC, Rx	← Rx OR AC	Rx: 40~7Fh
OR*	@HL	0010 1111 1000 0000	AC, @HL	← @HL OR AC	
ADCI	Ry, D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	CF
ADCI*	Ry, D	0011 0001 DDDD YYYY	AC, Ry	← Ry + D + CF	
SBCI	Ry, D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	
SBCI*	Ry, D	0011 0011 DDDD YYYY	AC, Ry	← Ry + DB + CF	
ADDI	Ry, D	0011 0100 DDDD YYYY	AC	← Ry + D	
ADDI*	Ry, D	0011 0101 DDDD YYYY	AC, Ry	← Ry + D	
SUBI	Ry, D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	
SUBI*	Ry, D	0011 0111 DDDD YYYY	AC, Ry	← Ry + DB + 1	
ADNI	Ry, D	0011 1000 DDDD YYYY	AC	← Ry + D	
ADNI*	Ry, D	0011 1001 DDDD YYYY	AC, Ry	← Ry + D	
ANDI	Ry, D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry, D	0011 1011 DDDD YYYY	AC, Ry	← Ry AND D	
EORI	Ry, D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry, D	0011 1101 DDDD YYYY	AC, Ry	← Ry EOR D	
ORI	Ry, D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry, D	0011 1111 DDDD YYYY	AC, Ry	← Ry OR D	
INC*	Rx	0100 0000 01XX XXXX	AC, Rx	← Rx + 1	CF, Rx: 40~7Fh
INC*	@HL	0100 0000 1000 0000	AC, @HL	← @HL + 1	CF
DEC*	Rx	0100 0001 01XX XXXX	AC, Rx	← Rx - 1	CF, Rx: 40~7Fh
DEC*	@HL	0100 0001 1000 0000	AC, @HL	← @HL - 1	CF
IPA	Rx	0100 0010 01XX XXXX	AC, Rx	← PortA (IOA4)	Rx: 40~7Fh
IPB	Rx	0100 0100 01XX XXXX	AC, Rx	← PortB (IOB4,3)	
IPC	Rx	0100 0111 01XX XXXX	AC, Rx	← PortC (IOC4~1)	
MAF	Rx	0100 1010 01XX XXXX	AC, Rx	← STS1	B3: CF B2: ZERO B1, B0: (Unused) Rx: 40~7Fh
MSB	Rx	0100 1011 01XX XXXX	AC, Rx	← STS2	B3: (Unused) B2: SCF2 (HRx) B1, B0: (Unused) Rx: 40~7Fh
MSC	Rx	0100 1100 01XX XXXX	AC, Rx	← STS3	B3: SCF7 (PDV) B2: PH15 B1, B0: (Unused) Rx: 40~7Fh
MCX	Rx	0100 1101 01XX XXXX	AC, Rx	← STS3X	B3: SCF9 (RFC)

Instruction		Machine Code	Function		Flag/Remark
					B2: SCF0 (APT) B1: SCF6 (TM2) B0: (Unused) Rx: 40~7Fh
MSD	Rx	0100 1110 01XX XXXX	AC, Rx	← STS4	B3: (Unused) B2: RFOVF B1, B0: (Unused) Rx: 40~7Fh
SR0	Rx	0101 0000 01XX XXXX	ACn, Rxn AC3, Rx3	← Rx (n+1) ← 0	Rx: 40~7Fh
SR1	Rx	0101 0001 01XX XXXX	ACn, Rxn AC3, Rx3	← Rx (n+1) ← 1	
SL0	Rx	0101 0010 01XX XXXX	ACn, Rxn AC0, Rx0	← Rx (n-1) ← 0	
SL1	Rx	0101 0011 01XX XXXX	ACn, Rxn AC0, Rx0	← Rx (n-1) ← 1	
DAA		0101 0100 0000 0000	AC	← BCD (AC)	
DAA*	Rx	0101 0101 01XX XXXX	AC, Rx	← BCD (AC)	Rx: 40~7Fh
DAA*	@HL	0101 0101 1000 0000	AC, @HL	← BCD (AC)	
DAS		0101 0110 0000 0000	AC	← BCD (AC)	
DAS*	Rx	0101 0111 01XX XXXX	AC, Rx	← BCD(AC)	Rx: 40~7Fh
DAS*	@HL	0101 0111 1000 0000	AC, @HL	← BCD(AC)	
LDS	Rx, D	0101 1DDD D1XX XXXX	AC, Rx	← D	Rx: 40~7Fh
LDH	Rx, @HL	0110 0000 01XX XXXX	AC, Rx	← H (T@HL)	
LDH*	Rx, @HL	0110 0001 01XX XXXX	AC, Rx HL	← H (T@HL) ← HL + 1	
LDL	Rx, @HL	0110 0010 01XX XXXX	AC, Rx	← L (T@HL)	
LDL*	Rx, @HL	0110 0011 01XX XXXX	AC, Rx HL	← L (T@HL) ← HL + 1	
MRF1	Rx	0110 0100 01XX XXXX	AC, Rx	← RFC3-0	
MRF2	Rx	0110 0101 01XX XXXX	AC, Rx	← RFC7-4	
MRF3	Rx	0110 0110 01XX XXXX	AC, Rx	← RFC11-8	
MRF4	Rx	0110 0111 01XX XXXX	AC, Rx	← RFC15-12	
STA	Rx	0110 1000 01XX XXXX	Rx	← AC	
STA	@HL	0110 1000 1000 0000	@HL	← AC	
LDA	Rx	0110 1100 01XX XXXX	AC	← Rx	Rx: 40~7Fh
LDA	@HL	0110 1100 1000 0000	AC	← @HL	
MRA	Rx	0110 1101 01XX XXXX	CF	← Rx3	Rx: 40~7Fh
MRW	@HL, Rx	0110 1110 01XX XXXX	AC, @HL	← Rx	
MWR	Rx, @HL	0110 1111 01XX XXXX	AC, Rx	← @HL	
MRW	Ry, Rx	0111 0YYY Y1XX XXXX	AC, Ry	← Rx	
MWR	Rx, Ry	0111 1YYY Y1XX XXXX	AC, Rx	← Ry	
JB0	X	1000 00XX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 10XX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 00XX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 10XX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 00XX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 10XX XXXX XXXX	PC	← X	if CF = 0

Instruction		Machine Code	Function		Flag/Remark
JZ	X	1011 00XX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 10XX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 00XX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 00XX XXXX XXXX	PC	← X	
RTS		1101 1000 0000 0000	PC	← STACK	CALL Return
SCC	X	1101 1001 0X10 0XXX	X6 = 1 X6 = 0 X2, 1, 0 = 001 X2, 1, 0 = 010 X2, 1, 0 = 100	: Cfq = BCLK : Cfq = PH0 : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1101 1010 00X0 0000	X5	: Enable SEF5	IOA4, X: 0 or 20h
SPA	X	1101 1100 000X X111	X4 X3	: Set A4 Pull-Low : Set A4 I/O	1:Output, 0: Input
SPB	X	1101 1101 000X XX01	X4 X3~0	: Set B4-3 Pull-Low : Set B4-3 I/O	1:Output, 0: Input
SPC	X	1101 1110 000X XXXX	X4 X3-0	: Set C4-1 Pull-Low /Low-Level-Hold : Set C4-1 I/O	1:Output, 0: Input
TM2	Rx	1110 0100 01XX XXXX	Timer2	← Rx & AC	Rx: 40~7Fh
TM2	@HL	1110 0101 0000 0000	Timer2	← T@HL	
TM2X	X	1110 011X XXXX XXXX	X8,7,6 = 111 X8,7,6 = 110 X8,7,6 = 101 X8,7,6 = 100 X8,7,6 = 011 X8,7,6 = 010 X8,7,6 = 001 X8,7,6 = 000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 0X0X X000	X6 X4 X3	: Enable HEF6 : Enable HEF4 : Enable HEF3	RFC TMR2 PDV
SIE*	X	1110 1001 0X0X X00X	X6 X4 X3 X0	: Enable IEF6 : Enable IEF4 : Enable IEF3 : Enable IEF0	RFC TMR2 PDV APT
PLC	X	1110 101X 0X0X X00X	X8 X6 X4 X3 X0	: Reset PH15~11 : Reset HRF6 : Reset HRF4 : Reset HRF3 : Reset HRF0	 RFC TMR2 PDV APT
SRF	X	1110 1100 00XX X0XX	X5 X4 X3 X1 X0	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RT Output : Enable RR Output	 ENX ETP ERR
SRE	X	1110 1101 0X00 0000	X6	: Enable SRF6	SRF6 (APT) X: 0 or 40h
SF		1111 0000 0000 0001	X0	: CF Set	CF
RF		1111 0100 0000 0001	X0	: CF Reset	CF
SF2	X	1111 1000 0000 0XXX	X2 X1 X0	: Close all Segments : Dis-ENX Set : Reload 2 Set	RSOFF DED RL2

Instruction		Machine Code	Function		Flag/Remark
RF2	X	1111 1001 0000 0XXX	X2 X1 X0	: Release Segments : Dis-ENX Reset : Reload 2 Reset	RSOFF DED RL2
ALM	X	1111 101X XXXX XXXX	X8, 7, 6 = 111 X8, 7, 6 = 100 X8, 7, 6 = 011 X8, 7, 6 = 010 X8, 7, 6 = 001 X8, 7, 6 = 000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

Symbol Description

AC	: Accumulator	D	: Immediate Data
ACn	: Accumulator bit n	PC	: Program Counter
X	: Address	CF	: Carry Flag
Rx	: Memory of address X	ZERO	: Zero Flag
Rxn	: Memory bit n of address X	HL	: Index Register
Ry	: Memory of working register Y	BCLK	: System clock, stop only in STOP condition
HRFn	: HALT Release Flag	IEFn	: Interrupt Enable Flag
HEFn	: HALT Release Enable Flag	SRFn	: STOP Release Enable Flag
PDV	: Pre-Divider	SCFn	: Start Condition Flag
Lz	: LCD Latch	Cch	: Clock Source of Chattering Detector
@HL	: Address of Index	Cfq	: Clock Source of Frequency Generator
@L	: Low address of Index	SEFn	: Switch Enable Flag
@H	: High address of Index	FREQ	: Frequency Generator setting Value
L (T@HL)	: Low Nibble of Index ROM	( )	: Content of Register
H (T@HL)	: High Nibble of Index ROM	TMR	: Timer Overflow Release Flag
T@HL	: Address of Index ROM	Ctm	: Clock Source of Timer
RFOVF	: RFC Overflow Flag		